

Figure 1
Different hint extension instructions.

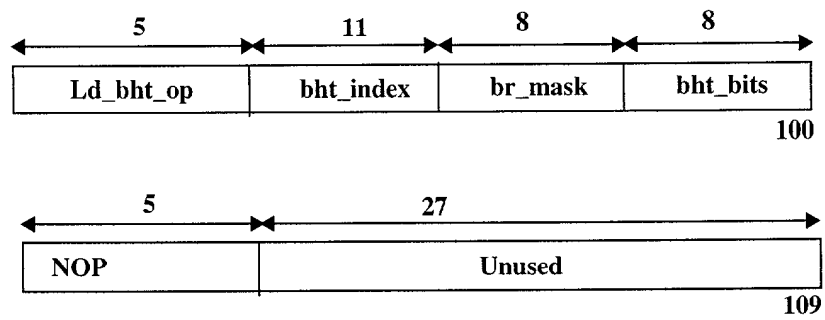


Figure 2
Overview of the Processor operation with Hint processor

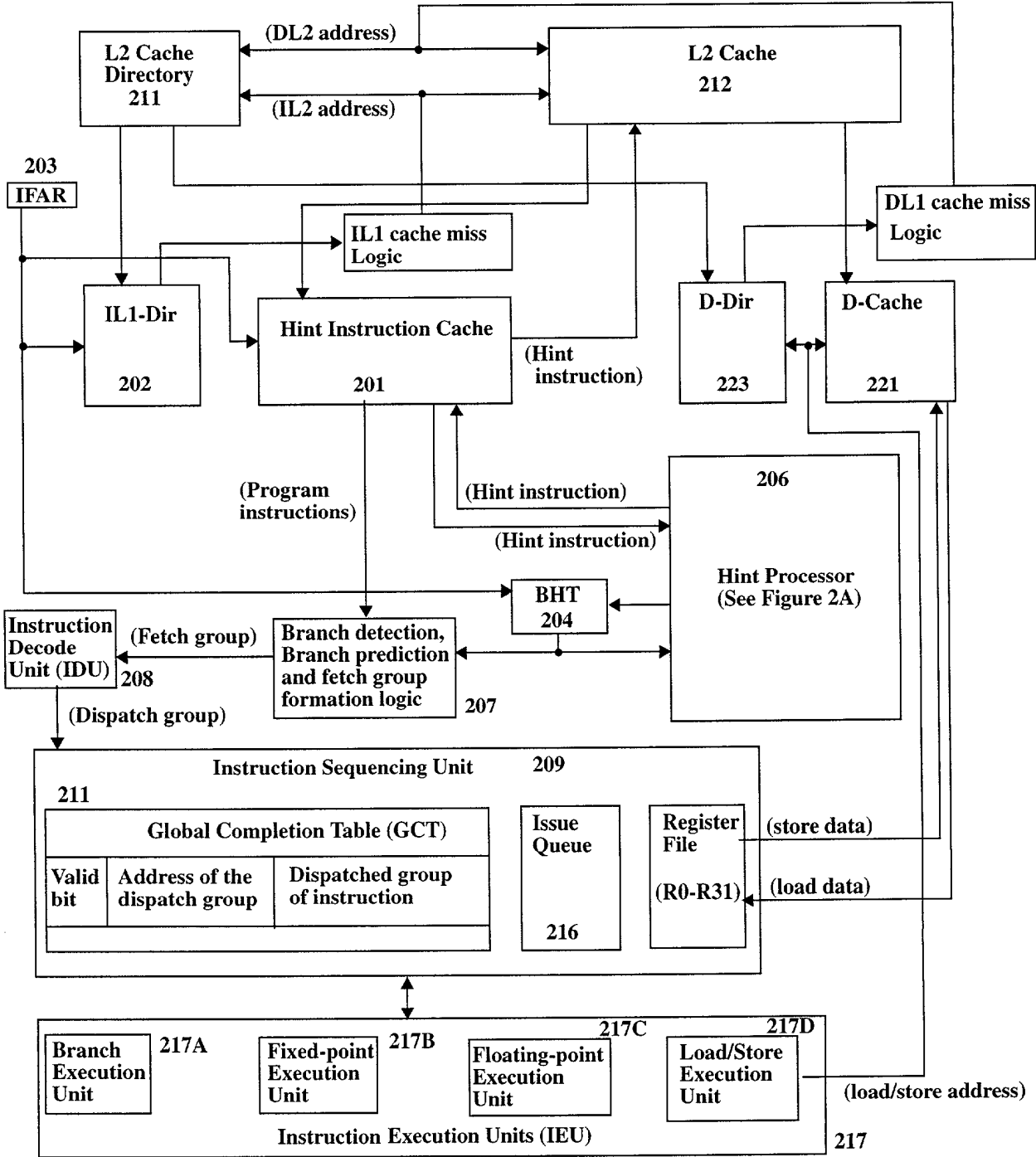


Figure 2A The Hint Processor

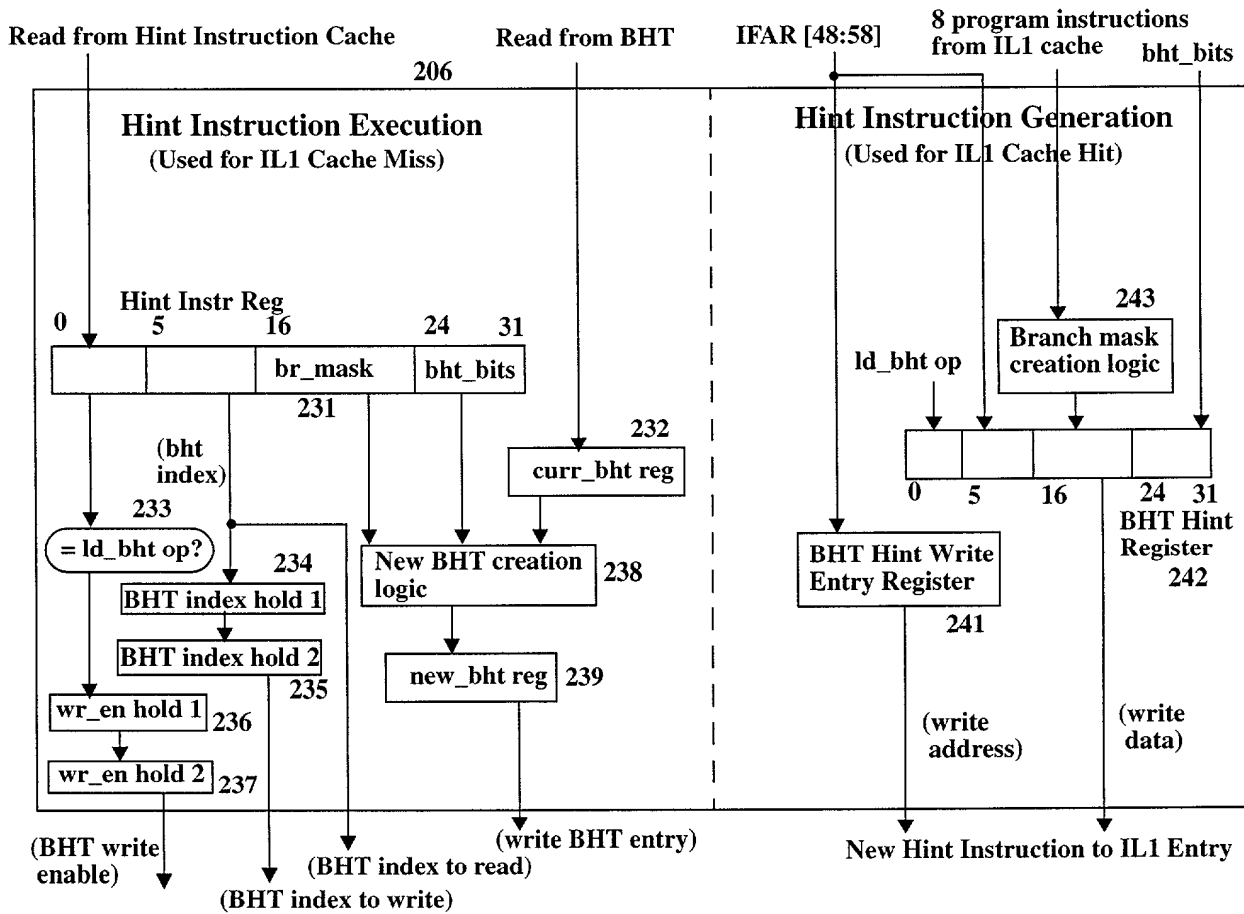


Figure 2B New BHT creation logic 238

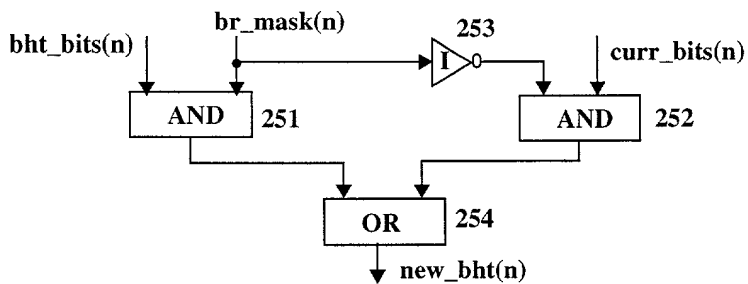


Figure 3

Overview of the Instruction Fetch Unit with Hint Processor

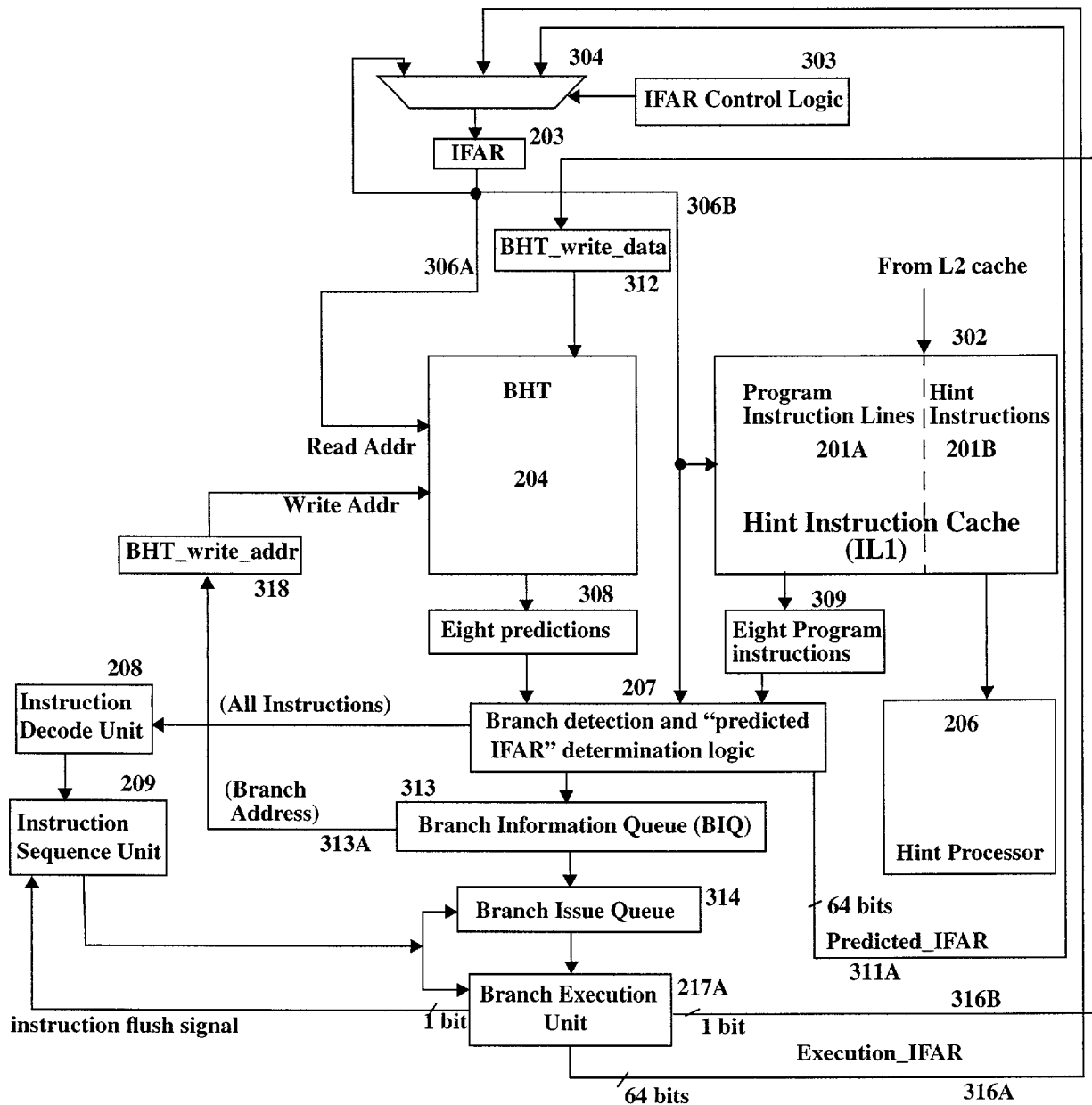
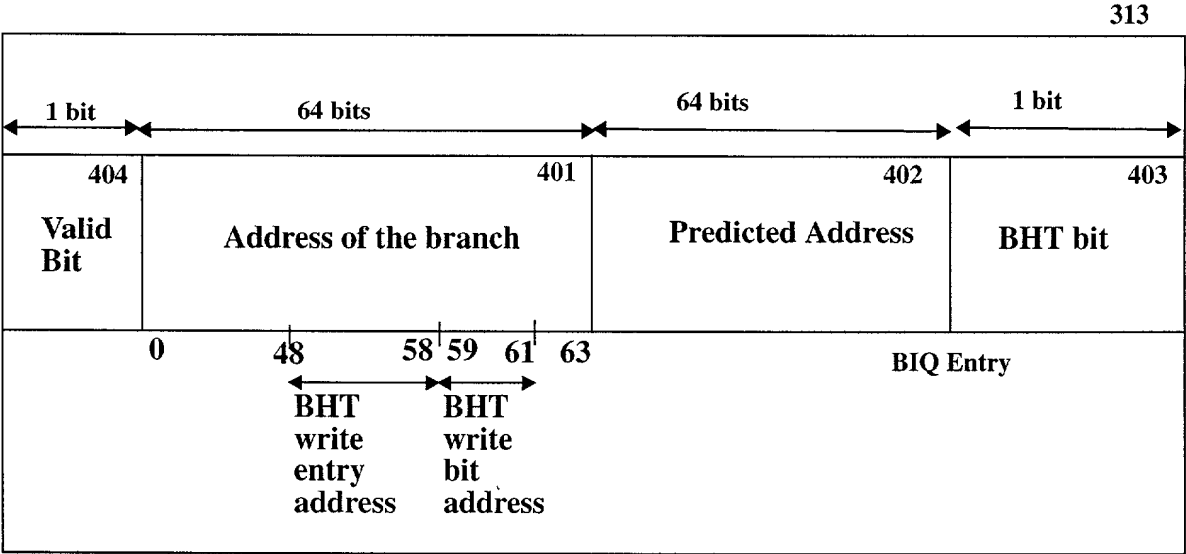
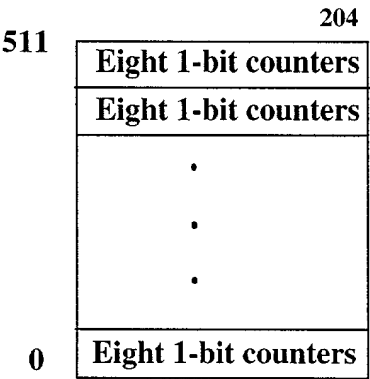


Figure 4



Branch Information Queue (BIQ)

Figure 5



BHT

Figure 6

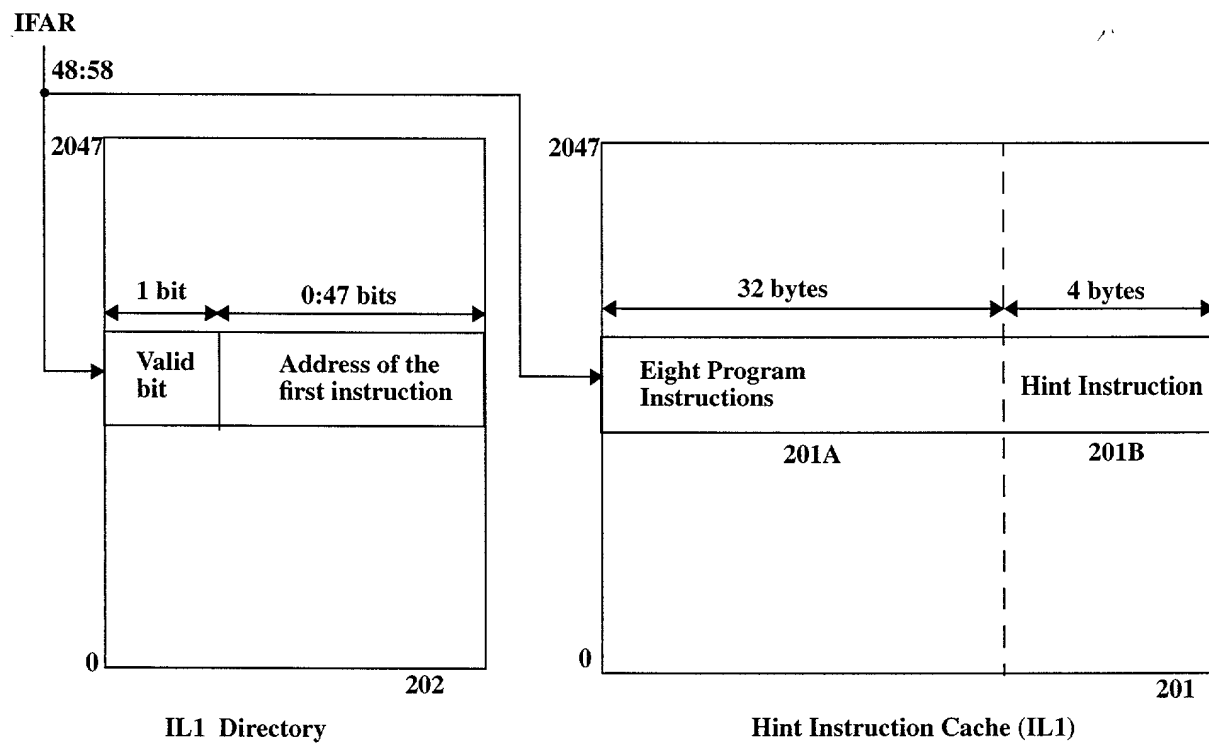
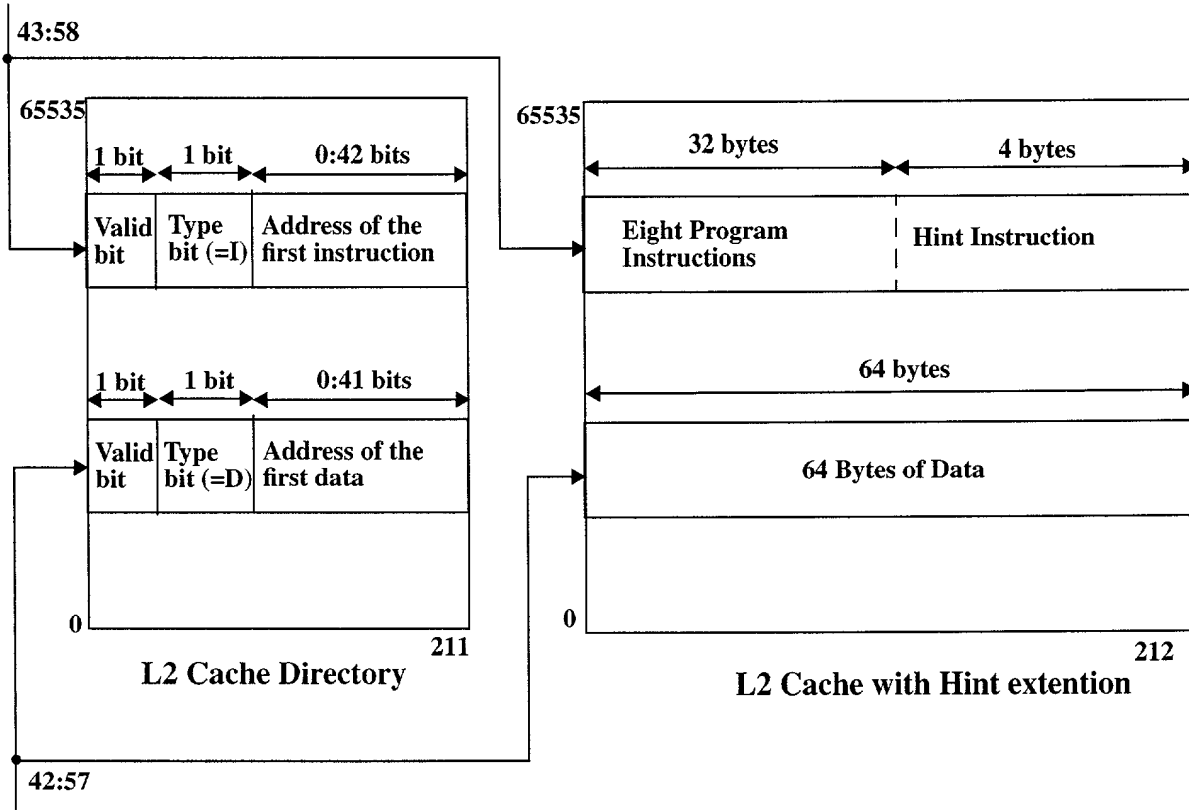


Figure 7

IL2 address



DL2 address

Figure 8

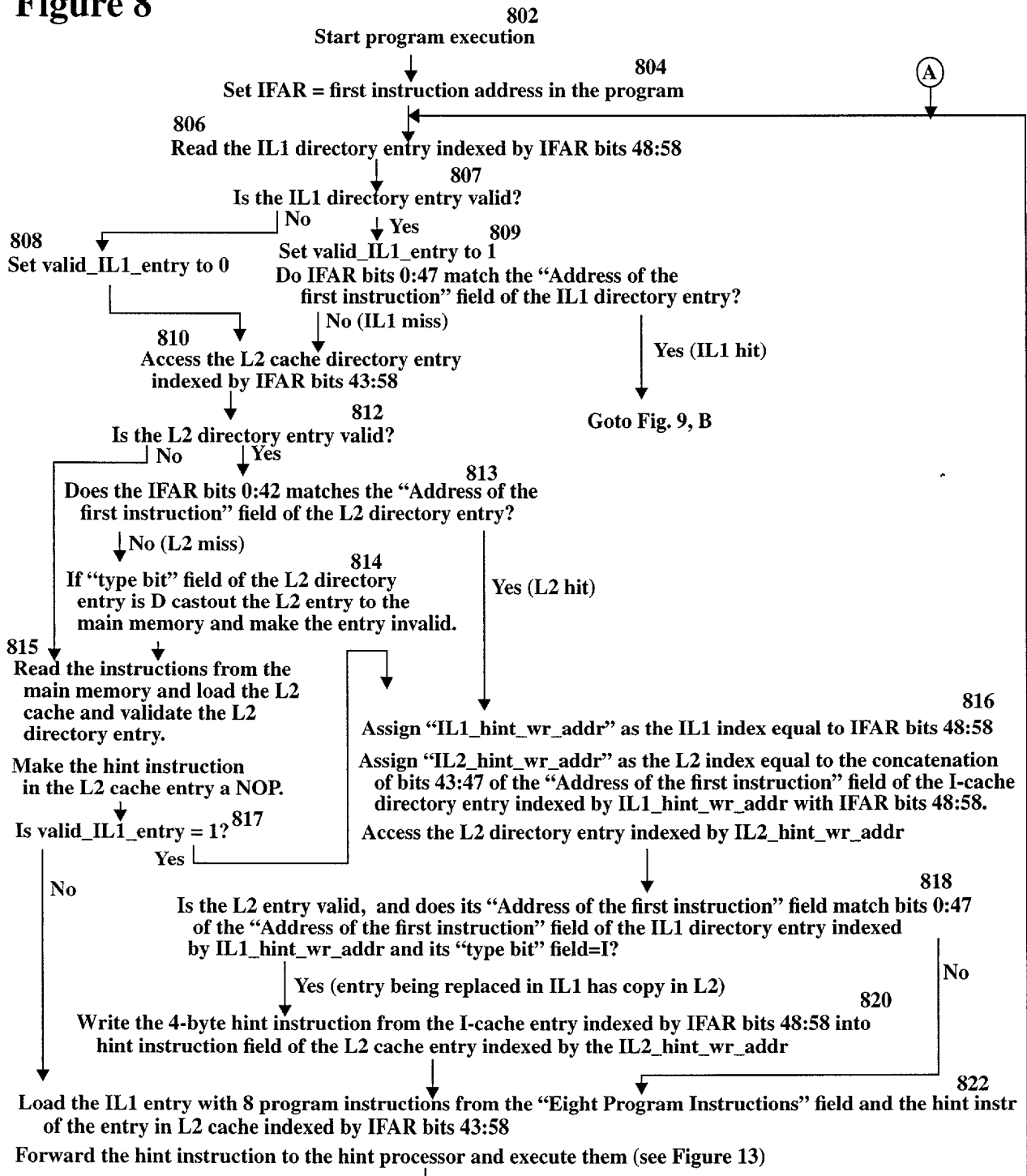


Figure 9

(B) From Figure 8.

901

Fetch the IL1 cache line into "Eight Program Instructions" register, and the associated hint instructions in the Hint Instruction register.

Access the BHT entry indexed by the IFAR bits 48:58, and fetch its BHT prediction bits into the "Eight Predictions" register.

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Use the IFAR bits 59:61 to locate "first instruction" in the "Eight Program Instructions" register. (Instructions before the "first instruction", if any, will be ignored).

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Is there any branch instruction in the "Eight Program Instructions" register at or after the "first instruction"?

Yes

No

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Designate a "fetch group" as the instructions from the "first instruction" to the end of the register. Set "Predicted_IFAR" to the address of the next sequential instruction after the "fetch group".

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In the hint processor, fill the BHT Hint register with the following: bits 0:4 with "ld_bht_op", bits 5:15 with IFAR bits 48:58, bits 16:23 with a 8-bit "branch mask" field containing a 1 in the positions where there is a branch and 0 in other positions, bits 24:31 with the 8-bit BHT prediction.

In the hint processor, store IFAR bits 48:58 in the BHT Hint Write Entry register

Store the content of the BHT Hint register in the Hint Instruction field in the IL1 Cache at the location in the BHT Hint Write Entry register

911

Is any branch indicated in the "Eight Predictions" register to be an unconditional branch or a conditional branch predicted taken?

Yes

No

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Set "Predicted_IFAR" to the target of the first of these branches and designates this branch as the "last instruction".

Set "Predicted_IFAR" to the address of the instruction next sequential to the last instruction fetched. Designate the last instruction in the "Eight Instructions" register as the "last instruction".

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All instructions between the "first instruction" and the "last instruction" forms the "fetch group".

For each branch in fetch group, obtain an invalid entry in the Branch Information Queue (BIQ), set its valid bit to 1 state and put:

the address of the branch in the "Address of the branch" field,

the branch target address in the "Predicted address" field if the branch is predicted taken or the sequential address in the "Predicted address" field if the branch is predicted not-taken,

if the branch is at position "n", store the n-th bit in the "Eight Predictions" register in the "BHT bit" field.

Place the branch in the branch issue queue for its subsequent execution.

926

Forward the fetch group to Instruction Decode Unit (IDU), see Figure 11.

Goto Figure 10, C

Figure 10

Next IFAR determination logic

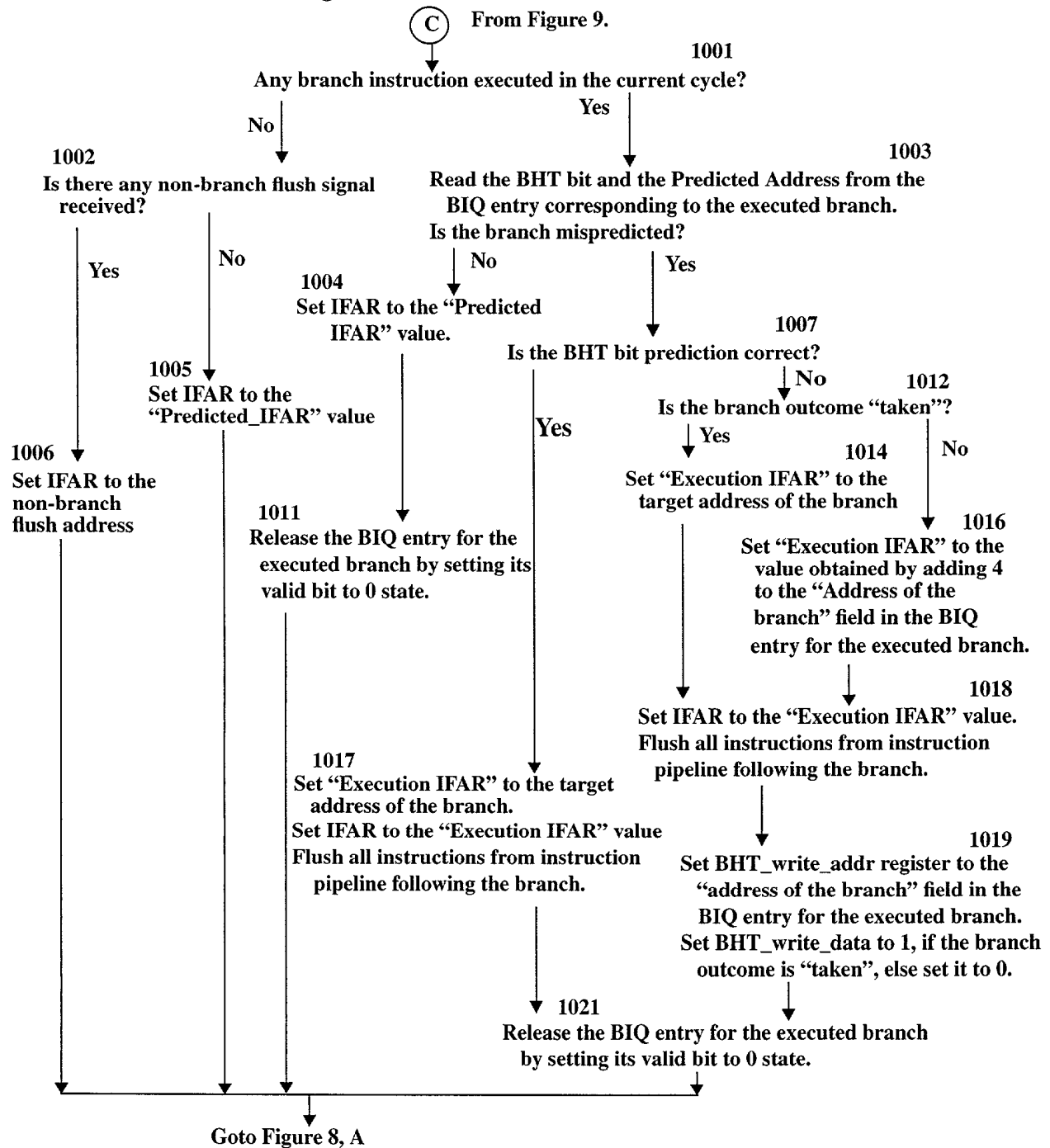


Figure 11
Instruction Decode and Dispatch

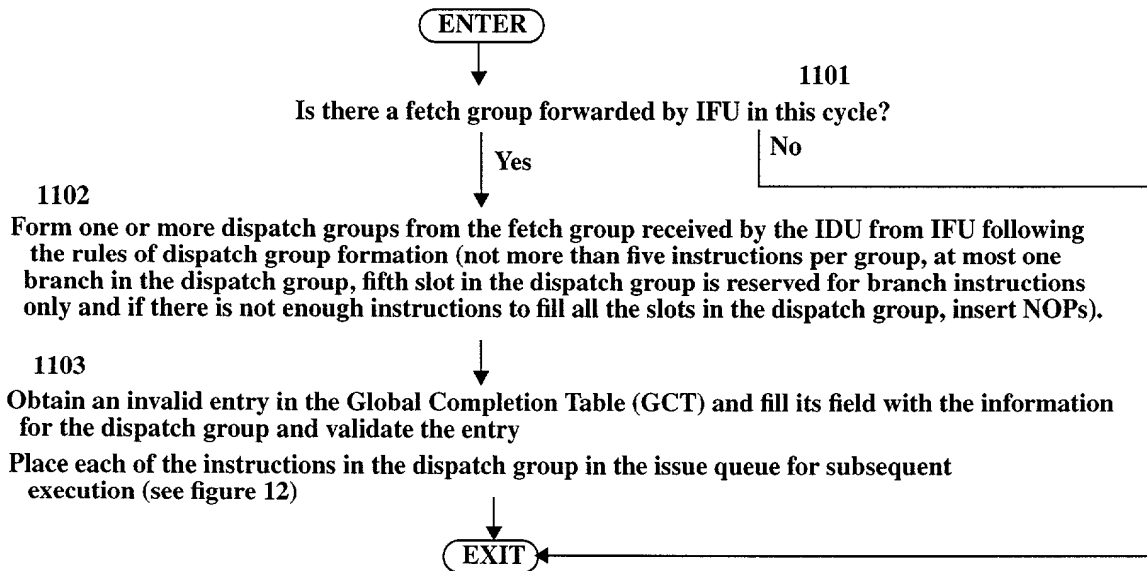


Figure 12

Instruction issue and instruction execution

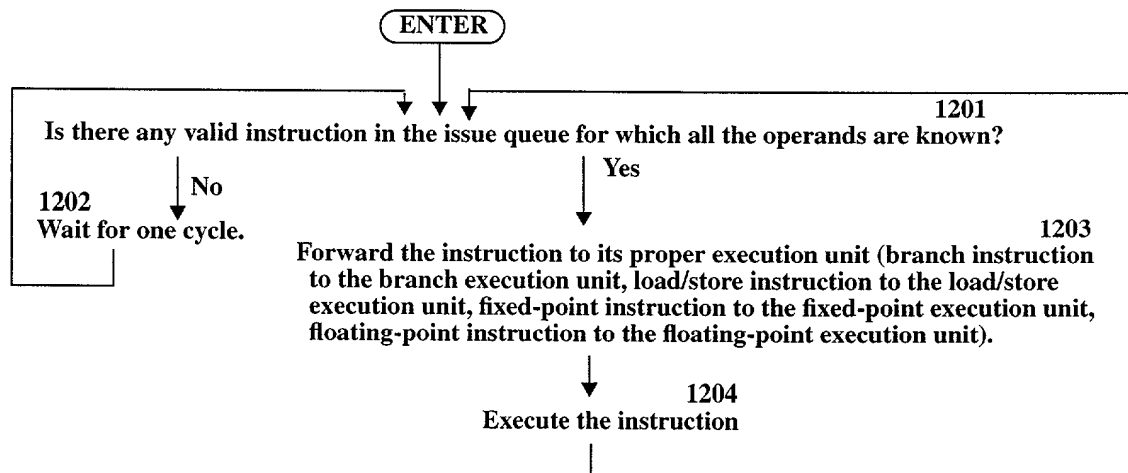


Figure 13

Execution in the Hint Processor for each IFAR cycle

